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Application Number	10/602,357
Filing Date	June-23, 2003
First Named Inventor	Robert Benware
Group Art Unit	2857
Examiner Name	Edward Raymond
Attorney Docket Number	81563 / 02-6301

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I am the:

☐ Applicant

☒ Assignee of Record of the entire interest

*Certificate under 37 CFR 3.73(b) is enclosed*

### SIGNATURE of Applicant or Assignee of Record

Name	SANDEEP JAGGI, Chief IP Counsel and Assistant Corporate Secretary, LSI Logic Corp.
Signature	<i>[Handwritten Signature]</i>
Date	1/5/05



11:09

LSI LOGIC LEGAL IP → 917037464000

NO. 304

0006

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE****In re Application of :**

Robert Benware

**Serial No. :**

10/602,357

**Group Art Un**

2857

**Filed :**

June 23, 2003

**Examiner:**

Raymond, Edward

**For :**Method of Screening Defects Using  
Low Voltage IDDQ Measurement**Atty Docket :**

81563 / 02-6301

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LSI Logic Corporation, a Delaware corporation, certifies that it is the assignee of the entire right, title and interest in the patent application.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of the undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Respectfully submitted,

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